CLAIMS

We claim:

1. A method for forming at least one high-k device, comprising the steps of:

providing a structure having a strained substrate formed thereover; the strained substrate comprising at least an uppermost strained-Si epi layer;;

forming at least one dielectric gate oxide portion over the strained substrate; the at least one dielectric gate oxide portion having a dielectric constant of greater than about 4.0; and

forming a device over each of the at least one dielectric gate oxide portion to complete formation of the least one high-k device.

2. The method of claim 1, wherein the at least one dielectric gate oxide portion is comprised of HfO_2, $HfSiO_4$, N-doped hafnium. $HfSiO_x$, ZrO_2, $ZrSiO_x$ or N-doped zirconium silicate.

3. The method of claim 1, wherein the structure is a silicon substrate or a germanium substrate.

4. The method of claim 1, wherein the uppermost strained-Si epi layer has a dislocation density of strained-Si epi of less than about $1E6/cm^2$.

5. The method of claim 1, wherein the strained substrate is comprised of only the uppermost strained-Si epi layer.

6. The method of claim 1, wherein the uppermost strained-Si epi layer having a thickness of from about 100 to 500Å.

7. The method of claim 1, wherein the uppermost strained-Si epi layer having a thickness of from about 150 to 300Å.

8. The method of claim 1, wherein the uppermost strained-Si epi layer having a thickness of from about 200 to 300Å.

9. The method of claim 1, wherein the strained substrate is comprised of the uppermost strained-Si epi layer, a middle relaxed $Si_{1-x}Ge_x$ layer and a lowermost graded $Si_{1-y}Ge_y$ layer.

10. The method of claim 1, wherein the strained substrate is comprised of the uppermost strained-Si epi layer, a middle relaxed $Si_{1-x}Ge_x$ layer and a lowermost graded $Si_{1-y}Ge_y$ layer; the uppermost strained-Si epi layer having a thickness of from about 100 to 500Å; the middle relaxed $Si_{1-x}Ge_x$ layer having a thickness of from about 1000 to 50,000Å; and the lowermost graded $Si_{1-y}Ge_y$ layer having a thickness of from about 2000 to 50,000Å.

11. The method of claim 1, wherein the strained substrate is comprised of the uppermost strained-Si epi layer, a middle relaxed $Si_{1-x}Ge_x$ layer where x is greater than 0 and less than about 0.50 and a lowermost graded $Si_{1-y}Ge_y$ layer where y is 0 or about 0 proximate structure and increases to about x proximate middle relaxed $Si_{1-x}Ge_x$ layer; wherein $x \geq y$.

12. The method of claim 1, wherein the strained substrate is comprised of the uppermost strained-Si epi layer, a middle $Si_{1-x}Ge_x$ layer and a lower silicon oxide layer.

13. The method of claim 1, wherein the strained substrate is comprised of the uppermost strained-Si epi layer, a middle $Si_{1-x}Ge_x$ layer and a lower silicon oxide layer; wherein the uppermost strained-Si epi layer has a thickness of from about 100 to 500Å, the middle $Si_{1-x}Ge_x$ layer has a thickness of from about 700 to 1200Å and the lower silicon oxide layer has a thickness of from about 800 to 2000Å.

14. The method of claim 1, wherein the strained substrate is comprised of the uppermost strained-Si epi layer over an upper relaxed $Si_{1-x}Ge_x$ layer over a graded $Si_{1-y}Ge_y$ layer over an epi layer over a lowermost relaxed $Si_{1-z}Ge_z$ layer; wherein $x \geq y \geq z$.

15. The method of claim 1, wherein the strained substrate is comprised of the uppermost strained-Si epi layer over an upper relaxed $Si_{1-x}Ge_x$ layer over a graded $Si_{1-y}Ge_y$ layer over an epi layer over a lowermost relaxed $Si_{1-z}Ge_z$ layer; the

uppermost strained-Si epi layer having a thickness of from about 100 to 500Å; the upper relaxed $Si_{1-x}Ge_x$ layer having a thickness of from about 1000 to 50,000Å; the graded $Si_{1-y}Ge_y$ layer having a thickness of from about 2000 to 50,000Å; the epi layer having a thickness of from about 20 to 500Å; and the lowermost relaxed $Si_{1-z}Ge_z$ layer having a thickness of from about 200 to 50,000Å.

16. The method of claim 1, wherein the strained substrate is comprised of the uppermost strained-Si epi layer over an upper relaxed $Si_{1-x}Ge_x$ layer over a graded $Si_{1-y}Ge_y$ layer over an epi layer over a lowermost relaxed $Si_{1-z}Ge_z$ layer; the uppermost strained-Si epi layer having a thickness of from about 150 to 300Å; the upper relaxed $Si_{1-x}Ge_x$ layer having a thickness of from about 2000 to 40,000Å; the graded $Si_{1-y}Ge_y$ layer having a thickness of from about 500 to 25,000Å; the epi layer having a thickness of from about 50 to 200Å; and the lowermost relaxed $Si_{1-z}Ge_z$ layer having a thickness of from about 500 to 25,000Å.

17. The method of claim 1, wherein the strained substrate is comprised of the uppermost strained-Si epi layer over an upper relaxed $Si_{1-x}Ge_x$ layer, where x is no less than y and less than about 0.50, over a graded $Si_{1-y}Ge_y$ layer, where y is no less than z proximate epi layer and increases to about x proximate upper relaxed $Si_{1-x}Ge_x$ layer, over an epi layer over a lowermost relaxed $Si_{1-z}Ge_z$ layer where z is greater than 0 and less than about 0.50.

18. The method of claim 1, wherein the at least one dielectric gate oxide portion is at least two dielectric gate oxide portions; at least one NMOS device is formed over at

least one of the at least two dielectric gate oxide portions; at least one PMOS device is formed over at least one of the at least two dielectric gate oxide portions; and the strained substrate is unitary under the at least one NMOS device and the at least one PMOS device.

19. The method of claim 1, wherein the at least one dielectric gate oxide portion 20, 30 being comprised of HfO_2 or $HfSiO_4$.

20. At least one high-k device, comprising:

a structure having a strained substrate formed thereover; the strained substrate comprising at least an uppermost strained-Si epi layer;

at least one dielectric gate oxide portion over the strained substrate; the at least one dielectric gate oxide portion having a dielectric constant of greater than about 4.0; and

a device over each of the at least one dielectric gate oxide portion to complete the least one high-k device.

21. The structure of claim 20, wherein the at least one dielectric gate oxide portion is comprised of HfO_2, $HfSiO_4$, N-doped hafnium. $HfSiO_x$, ZrO_2, $ZrSiO_x$ or N-doped zirconium silicate.

22. The device of claim 20, wherein the structure is a silicon substrate or a germanium substrate.

23. The device of claim 20, wherein the uppermost strained-Si epi layer has a dislocation density of strained-Si epi of less than about 1E6/cm^2.

24. The device of claim 20, wherein the strained substrate is comprised of only the uppermost strained-Si epi layer.

25. The device of claim 20, wherein the strained substrate is comprised of only the uppermost strained-Si epi layer having a thickness of from about 100 to 500Å.

26. The device of claim 20, wherein the strained substrate is comprised of only the uppermost strained-Si epi layer having a thickness of from about 150 to 300Å.

27. The device of claim 20, wherein the strained substrate is comprised of only the uppermost strained-Si epi layer having a thickness of from about 200 to 300Å.

28. The device of claim 20, wherein the strained substrate is comprised of the uppermost strained-Si epi layer, a middle relaxed $Si_{1-x}Ge_x$ layer and a lowermost graded $Si_{1-y}Ge_y$ layer.

29. The device of claim 20, wherein the strained substrate is comprised of the uppermost strained-Si epi layer, a middle relaxed $Si_{1-x}Ge_x$ layer and a lowermost graded $Si_{1-y}Ge_y$ layer; the uppermost strained-Si epi layer having a thickness of from about 100 to 500Å; the middle relaxed $Si_{1-x}Ge_x$ layer having a thickness of

from about 1000 to 50,000Å; and the lowermost graded $Si_{1-y}Ge_y$ layer having a thickness of from about 200 to 50,000Å.

30. The device of claim 20, wherein the strained substrate is comprised of the uppermost strained-Si epi layer, a middle relaxed $Si_{1-x}Ge_x$ layer where x is greater than 0 and less than about 0.50 and a lowermost graded $Si_{1-y}Ge_y$ layer where y is 0 or about 0 proximate structure and increases to about x proximate middle relaxed $Si_{1-x}Ge_x$ layer, wherein $x \geq y$.

31. The device of claim 20, wherein the strained substrate is comprised of the uppermost strained-Si epi layer, a middle $Si_{1-x}Ge_x$ layer and a lower silicon oxide layer.

32. The device of claim 20, wherein the strained substrate is comprised of the uppermost strained-Si epi layer, a middle $Si_{1-x}Ge_x$ layer and a lower silicon oxide layer; wherein the uppermost strained-Si epi layer has a thickness of from about 100 to 500Å, the middle $Si_{1-x}Ge_x$ layer has a thickness of from about 700 to 1200 and the lower silicon oxide layer has a thickness of from about 800 to 2000Å.

33. The device of claim 20, wherein the strained substrate is comprised of the uppermost strained-Si epi layer over an upper relaxed $Si_{1-x}Ge_x$ layer over a graded $Si_{1-y}Ge_y$ layer over an epi layer over a lowermost relaxed $Si_{1-z}Ge_z$ layer; wherein $x \geq y \geq z$.

34. The device of claim 20, wherein the strained substrate is comprised of the uppermost strained-Si epi layer over an upper relaxed $Si_{1-x}Ge_x$ layer over a graded $Si_{1-y}Ge_y$ layer over an epi layer over a lowermost relaxed $Si_{1-z}Ge_z$ layer; the uppermost strained-Si epi layer having a thickness of from about 100 to 500Å; the upper relaxed $Si_{1-x}Ge_x$ layer having a thickness of from about 1000 to 50,000Å; the graded $Si_{1-y}Ge_y$ layer having a thickness of from about 2000 to 50,000Å; the epi layer having a thickness of from about 20 to 500Å; and the lowermost relaxed $Si_{1-z}Ge_z$ layer having a thickness of from about 200 to 50,000Å.

35. The device of claim 20, wherein the strained substrate is comprised of the uppermost strained-Si epi layer over an upper relaxed $Si_{1-x}Ge_x$ layer over a graded $Si_{1-y}Ge_y$ layer over an epi layer over a lowermost relaxed $Si_{1-z}Ge_z$ layer; the uppermost strained-Si epi layer having a thickness of from about 150 to 300Å; the upper relaxed $Si_{1-x}Ge_x$ layer having a thickness of from about 2000 to 40,000Å; the graded $Si_{1-y}Ge_y$ layer having a thickness of from about 500 to 25,000Å; the epi layer having a thickness of from about 50 to 200Å; and the lowermost relaxed $Si_{1-z}Ge_z$ layer having a thickness of from about 500 to 25,000Å.

36. The device of claim 20, wherein the strained substrate is comprised of the uppermost strained-Si epi layer over an upper relaxed $Si_{1-x}Ge_x$ layer, where x is no less than y and less than about 0.50, over a graded $Si_{1-y}Ge_y$ layer, where y is no less than z proximate epi layer and increases to about x proximate upper relaxed $Si_{1-x}Ge_x$ layer, over an epi layer over a lowermost relaxed $Si_{1-z}Ge_z$ layer where z is greater than 0 and less than about 0.50.

37. The device of claim 20, wherein the at least one dielectric gate oxide portion being comprised of HfO_2 or $HfSiO_4$.

38. The structure of claim 20, wherein the strained substrate further includes a relaxed $Si_{1-y}Ge_y$ layer having a thickness of from about 200 to 30,000Å under the uppermost strained-Si epi layer; a constant $Si_{1-y}Ge_y$ layer having a thickness of from about 200 to 20,000Å under the relaxed $Si_{1-y}Ge_y$ layer; a silicon epi layer having a thickness of from about 20 to 500Å under the constant $Si_{1-y}Ge_y$ layer; and a constant $Si_{1-z}Ge_z$ layer having a thickness of from about 200 to 20,000Å under the silicon epi layer; and the uppermost strained-Si epi layer having a thickness of from about 20 to 500Å.

39. The structure of claim 20, wherein the strained substrate further includes a relaxed $Si_{1-y}Ge_y$ layer having a thickness of from about 300 to 5000Å under the uppermost strained-Si epi layer; a constant $Si_{1-y}Ge_y$ layer having a thickness of from about 300 to 5000Å under the relaxed $Si_{1-y}Ge_y$ layer; a silicon epi layer having a thickness of from about 50 to 300Å under the constant $Si_{1-y}Ge_y$ layer; and a constant $Si_{1-z}Ge_z$ layer having a thickness of from about 300 to 5000Å under the silicon epi layer; and the uppermost strained-Si epi layer having a thickness of from about 50 to 300Å.

40. The structure of claim 20, wherein the at least one dielectric gate oxide portion is comprised of HfO_2 or $HfSiO_4$.

41. The structure of claim 20, wherein the strained substrate further includes a relaxed $Si_{1-y}Ge_y$ layer under the uppermost strained-Si epi layer; a constant $Si_{1-y}Ge_y$ layer under the relaxed $Si_{1-y}Ge_y$ layer; a silicon epi layer under the constant $Si_{1-y}Ge_y$ layer; and a constant $Si_{1-z}Ge_z$ layer under the silicon epi layer; wherein the uppermost relaxed-Si epi layer is comprised of $Si_{1-x}Ge_x$ wherein x is constant or graded.